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REMARKS

Claims 1-14 are pending in the application, with claims 1-6 having been withdrawn from consideration.

Claims 7 and 9-13 are amended in order to more particularly point out, and distinctly claim the subject matter to which the applicant regards as his invention. It is believed that this Amendment is fully responsive to the Office Action dated **November 6, 2002**.

Objection to the Drawings

The drawings have been objected to for failing to illustrate "a plurality of convex regions". Claims 7 and 9-13 have been amended to substitute the term "insulating" for the term "convex". As illustrated in figures 2a, 2b, 4a, 4b, 4c 6a, 6b, 7a, 7b, and 7c, a plurality of insulating regions (21a) are illustrated in these figures. Therefore, withdrawal of the objection to figures is respectfully requested.

Claim Rejections under 35 USC §112, First Paragraph

Claims 7-13 are rejected under 35 USC §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains to make and/or use the invention.

Specifically, the Examiner asserts that the terms "convex regions" and "recess area ratio" are not supported by the specification. The term "convex regions" has been replaced with the term "insulating regions" which, as previously discussed, finds support in the figures and the specification.

The recess area ratio of X is equal to Sr/St, where Sr is a square measurement of the recess formed in X and St is a total square measurement of X. The embodiment is shown in Fig. 2A and described on page 10, line 15 through page 11, line 17, which corresponds to the particular case in which the recess area ratio in the near wiring area is equal to 100%.

The near wiring area, of the first frame area, and of the second frame area of claim 7 corresponds to the area 27b, the first frame area 27a and the second frame area 27c, shown in Fig. 2A, respectively. In the embodiment shown in Fig. 2A, there is no insulating region 21a in the near wiring area 27b. Accordingly, the recess area ratio in the near wiring area 27b is equal to 100%. There are some insulating regions 21a in the second frame area 27c. Accordingly, the recess ratio in the second frame area 27c is smaller than 100%. Namely, the recess area ratio in the near wiring area 27b is larger than the recess ratio in the second frame area 27c.

Therefore, withdrawal of the rejection of Claims 7-13 under 35 USC §112, first paragraph, is respectfully requested.

Claim Rejections under 35 USC §112, Second Paragraph

Claim 11 is rejected under 35 USC §112, second paragraph, as being indefinite. Specifically, the Examiner asserts that "the via hole" lacks antecedent basis. Taking the Examiner's comments into consideration, applicant has amended claim 11 to overcome this rejection. Therefore, withdrawal of the rejection of claim 11 under 35 USC § 112, second paragraph, is respectfully requested.

Claim Rejections under 35 USC §102

Claims 7-13 are rejected under 35 USC §102(e) as being anticipated by Harada et al. (U.S. Patent No. 6,417,575 B2).

Harada et al. describes a semiconductor device and method of manufacturing the same which includes a pad electrode and main electrode layer. This device includes a first interlayer insulating film (7) a first intra-layer insulating film (11). Please note that the pad portion of this device is wider than the wiring portion.

The present invention is a semiconductor device having a pad capable of suppressing excess current concentration. As illustrated in Fig. 2a, the pad includes a large number of insulating regions (21a) in which specific ratios of dimensions are followed. For example, W1 corresponds to the width of the wiring portion (25). The pad is divided into three portions. A first frame area (27a) having a width of L1. A second frame area (27c) has a width L2 and contains several insulating regions (21a). A central area (27d) is contained in the middle of the pad and may contain a via hole. The width L1 of the first frame area (27 a) is equal to or wider than the distance between insulating regions (21a). As illustrated in Fig. 2A, the total width of pad (27) corresponds to 2 x W2 + n x W3 as discussed on page 11, line 22 of the specification, W1 corresponds to the distance L1 and W3 corresponds to the distance P2. As discussed in the example provided on page 12, lines 4-11, W1 is larger than the distance L1 and the ratio L1/W1 is 30 percent or higher.

Harada et al. does not describe or suggest a pad composed of three regions having a number of insulating regions (21a) contained and a second frame area (27c). Further, the width of the first frame area (27a) is not larger than a recess area ratio in the second frame area (27c). Therefore, the

present invention patentably distinguishes over Harada et al.

The recess area ratio in a near wiring area is defined as (the square measurement of the recess in the near wiring area)/(the total square measurement of the near wiring area). The recess area ratio in a second frame is defined by (the square measurement of the recess in the second frame area)/(the total square measurement of the recess in the second frame area).

Specifically, independent claim 7 patentably distinguishes over the prior are relied upon, by reciting,

> "A semiconductor device comprising: a semiconductor substrate; a first interlayer insulating film made of insulating material and formed on the semiconductor substrate; a first intra-layer insulating film made of insulating material and formed on the first interlayer insulating film, the first intra-layer insulating film being formed with a recess reaching a bottom of the first intra-layer insulating film, the recess having a pad part and a wiring part continuous with the pad part, the pad part having a width wider than a width of the wiring part, a plurality of insulating regions being protruded from the bottom of the pad part, and the recess being formed so that the insulating regions are disposed in such a manner that a recess area ratio in a near wiring area superposed upon an extended area of the wiring part into the pad part, within a first frame area having as an outer periphery an outer periphery of the pad part and having a first width, becomes larger than a recess area ratio in a second frame area having as an outer periphery an inner periphery of the first frame area and having a second width, wherein the recess area ratio in the near wring area is a square measurement of the recess in the near wiring area divided by a total square measurement of the near wiring area and the recess area ratio in the second frame area is a square measurement of the recess in the second frame area divided by a total square measurement of the second frame area; a first pad filled in the pad part of the recess; and a wiring filled in the wiring part of the recess." (Emphasis Added)

Therefore, withdrawal of the rejection of Claims 7-13 under 35 USC §102(e) as being anticipated by Harada et al. (U.S. Patent No. 6,417,575 B2) is respectfully requested.

New Claim

New Claim 14 is added to the application. As shown in Fig. 1, the pad 27 in the first wiring layer connects with the wiring pattern 25. However, the pads in the second, third and fourth wiring layers do not connect with a wiring pattern in the same wiring layer. The pad of the new claim corresponds to the pads in the second, third and fourth wiring layers. For example, the pad in the second wiring layer connects with the wiring pattern in the first wiring layer via a plug 36 between the first and the second wiring layers.

When the wire is bonded to the pad, the pad becomes stressed. The stress is easy to concentrate to the periphery region (the first frame area) of the pad. The pad as recited in claim 14 can withstand the stress concentration because the recess area in the first frame area is large.

Claim 14 patentably distinguishes over the prior are relied upon, by reciting,

> "A semiconductor device comprising: a semiconductor substrate; a first interlayer insulating film made of insulating material and formed on the semiconductor substrate; a first intra-layer insulating film made of insulating material and formed on the first interlayer insulating film, the first intra-layer insulating film being formed with a recess reaching a bottom of the first intra-layer insulating film, the recess having a pad part, a plurality of insulating regions being protruded from the bottom of the pad part, and the recess being formed so that the insulating regions are disposed in such a manner that a recess area ratio in a first frame area having as an outer periphery an outer periphery of the pad part and having a first width, becomes larger than a recess area ratio in a second frame area having as an outer periphery an inner periphery of the first frame area and having a second width, wherein the recess area ratio in the first frame area is a square measurement of the recess in a near wiring area divided by a total square measurement of the near wiring area and the recess area ratio in the second frame area is a square measurement of the recess in the second frame area divided by a total square measurement of the second frame area; and a first pad filled in the pad part of the recess." (Emphasis Added)

Therefore, allowance of new claim 14 is respectfully requested.

Conclusion

In view of the aforementioned amendments and accompanying remarks, claims 7 and 9-13, as amended, are in condition for allowance, which action, at an early date, is requested.

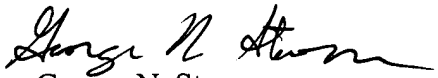
If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN & HATTORI, LLP



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Enclosures: Version with markings to show changes made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE 10/050,171

IN THE CLAIMS:

Please amend claims 7 and 9-13 as follows:

7. (Amended) A semiconductor device comprising:

a semiconductor substrate;

a first interlayer insulating film made of insulating material and formed on the semiconductor substrate;

a first intra-layer insulating film made of insulating material and formed on the first interlayer insulating film, the first intra-layer insulating film being formed with a recess reaching a bottom of the first intra-layer insulating film, the recess having a pad part and a wiring part continuous with the pad part, the pad part having a width wider than a width of the wiring part, a plurality of [convex] insulating regions being [left in] protruded from the bottom of the pad part, and the recess being formed so that the [convex] insulating regions are disposed in such a manner that a recess area ratio in a near wiring area superposed upon an extended area of the wiring part into the pad part, within a first frame area having as an outer periphery an outer periphery of the pad part and having a first width, becomes larger than a recess area ratio in a second frame area having as an outer periphery an inner periphery of the first frame area and having a second width, wherein the recess area ratio in the near wring area is a square measurement of the recess in the near wiring area divided by a total square measurement of the near wiring area and the recess area ratio in the second frame area is a square measurement of the recess in the second frame area

divided by a total square measurement of the second frame area;

a first pad filled in the pad part of the recess; and

a wiring filled in the wiring part of the recess.

9. (Amended) A semiconductor device according to claim 7, wherein the [convex] insulating regions are not disposed in the near wiring area.

10. (Amended) A semiconductor device according to claim 7, wherein the [convex] insulating regions are not disposed in a central area on an inner side of the second frame area.

11. (Amended) A semiconductor device according to claim [7] 8, wherein the via hole are included in the first pad as viewed along a direction parallel to a substrate normal.

12. (Amended) A semiconductor device according to claim 7, wherein the [convex] insulating regions are disposed regularly in the second frame area along a first direction at a first pitch, and a width of the first frame area along the first direction is equal to or wider than the first pitch.

13. (Amended) A semiconductor device according to claim 8, further comprising a conductive wire wire-bonded to the second pad, wherein the [convex] insulating regions are not

disposed in a central area on an inner side of the second frame area, the via hole are disposed in the central area, and a contact area between the conductive wire and the second pad extends to an area on an outer side of the via hole as viewed along a direction parallel to a substrate normal.